

DATA SHEET

74LVC2245A

Octal transceiver with direction pin,
30 Ω series termination resistors;
5 V tolerant input/output; 3-state

Product specification
Supersedes data of 2002 Jun 10

2003 Nov 17

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FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Integrated 30 Ω termination resistors
- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to $+85$ $^{\circ}\text{C}$ and -40 to $+125$ $^{\circ}\text{C}$.

DESCRIPTION

The 74LVC2245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC2245A is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The 74LVC2245A features an output enable ($\overline{\text{OE}}$) input for easy cascading and a send/receive (DIR) input for direction control. $\overline{\text{OE}}$ controls the outputs so that the buses are effectively isolated.

The 74LVC2245A is designed with 30 Ω series termination resistors in both HIGH and LOW output stages to reduce line noise.

QUICK REFERENCE DATA

GND = 0 V; $T_{\text{amb}} = 25$ $^{\circ}\text{C}$; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{\text{PHL}}/t_{\text{PLH}}$	propagation delay A_n to B_n , B_n to A_n	$C_L = 50$ pF; $V_{\text{CC}} = 3.3$ V	3.6	ns
C_I	input capacitance		4.0	pF
C_{PD}	power dissipation capacitance per buffer	$V_{\text{CC}} = 3.3$ V; notes 1 and 2	13	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \Sigma(C_L \times V_{\text{CC}}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{\text{CC}}^2 \times f_o)$ = sum of the outputs.

2. The condition is $V_I = \text{GND}$ to V_{CC} .

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC2245AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVC2245ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC2245APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC2245ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

FUNCTION TABLE

See note 1.

INPUT		INPUT/OUTPUT	
$\overline{\text{OE}}$	DIR	A _n	B _n
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

Note

1. H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

PINNING

PIN	SYMBOL	DESCRIPTION
1	DIR	direction control input
2	A0	data input/output
3	A1	data input/output
4	A2	data input/output
5	A3	data input/output
6	A4	data input/output
7	A5	data input/output
8	A6	data input/output
9	A7	data input/output
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	B7	data input/output
12	B5	data input/output
13	B5	data input/output
14	B4	data input/output
15	B3	data input/output
16	B2	data input/output
17	B1	data input/output
18	B0	data input/output
19	$\overline{\text{OE}}$	output enable input (active LOW)
20	V _{CC}	supply voltage

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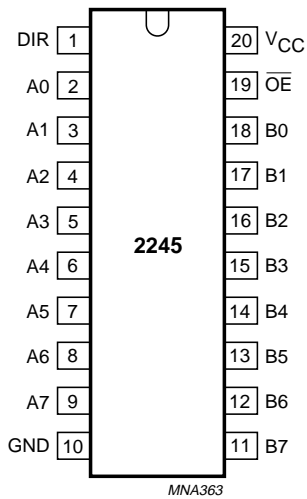
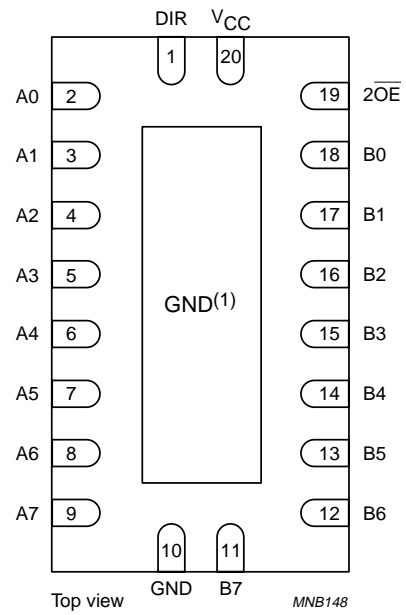


Fig.1 Pin configuration SO20 and (T)SSOP20.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN20.

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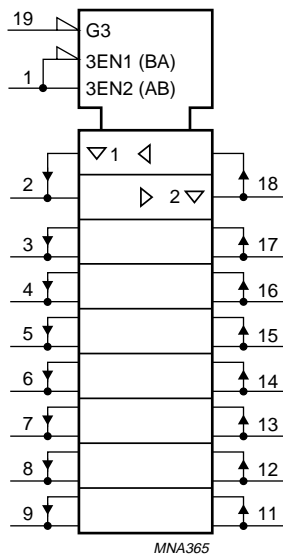


Fig.3 Logic symbol (IEEE/IEC).

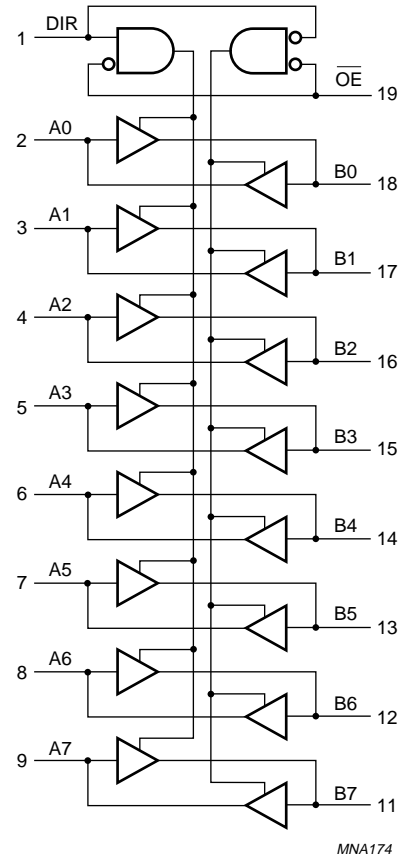


Fig.4 Logic symbol.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	ambient temperature		-40	+125	$^{\circ}\text{C}$
t_r, t_f	input rise and fall times	$V_{CC} = 1.2$ to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	-	-50	mA
V_I	input voltage	note 1	-0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	± 50	mA
V_O	output voltage	output HIGH or LOW state; note 1	-0.5	$V_{CC} + 0.5$	V
		output 3-state; note 1	-0.5	+6.5	V
I_O	output source or sink current	$V_O = 0$ to V_{CC}	-	± 50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	± 100	mA
T_{stg}	storage temperature		-65	+150	$^{\circ}\text{C}$
P_{tot}	power dissipation	$T_{amb} = -40$ to $+125$ $^{\circ}\text{C}$; note 2	-	500	mW

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO20 packages: above 70 $^{\circ}\text{C}$ derate linearly with 8 mW/K.
For SSOP20 and TSSOP20 packages: above 60 $^{\circ}\text{C}$ derate linearly with 5.5 mW/K.
For DHVQFN20 packages: above 60 $^{\circ}\text{C}$ derate linearly with 4.5 mW/K.

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DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V _{IL}	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μ A I _O = -6 mA I _O = -12 mA	2.7 to 3.6	V _{CC} - 0.2	V _{CC}	–	V
			2.7	V _{CC} - 0.5	–	–	V
			3.0	V _{CC} - 0.8	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μ A I _O = 6 mA I _O = 12 mA	2.7 to 3.6	–	0	0.2	V
			2.7	–	–	0.4	V
			3.0	–	–	0.55	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	–	\pm 0.1	\pm 5	μ A
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND	3.6	–	\pm 0.1	\pm 5	μ A
I _{off}	power off leakage supply	V _I or V _O = 5.5 V	0.0	–	\pm 0.1	\pm 10	μ A
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	–	0.1	10	μ A
Δ I _{CC}	additional quiescent supply current per pin	V _I = V _{CC} - 0.6 V; I _O = 0	2.7 to 3.6	–	5	500	μ A

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V _{IL}	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μ A	2.7 to 3.6	V _{CC} - 0.3	–	–	V
		I _O = -6 mA	2.7	V _{CC} - 0.65	–	–	V
		I _O = -12 mA	3.0	V _{CC} - 1	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μ A	2.7 to 3.6	–	–	0.3	V
		I _O = 6 mA	2.7	–	–	0.6	V
		I _O = 12 mA	3.0	–	–	0.8	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	–	–	\pm 20	μ A
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND	3.6	–	–	\pm 20	μ A
I _{off}	power off leakage supply	V _I or V _O = 5.5 V	0.0	–	–	\pm 20	μ A
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	–	–	40	μ A
Δ I _{CC}	additional quiescent supply current per pin	V _I = V _{CC} - 0.6 V; I _O = 0	2.7 to 3.6	–	–	5000	μ A

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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AC CHARACTERISTICSGND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay An to Bn; Bn to An	see Figs 5 and 7	1.2	–	26	–	ns
			2.7	1.5	4.0	7.3	ns
			3.0 to 3.6	1.5	3.6 ⁽¹⁾	6.3	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to An; OE to Bn	see Figs 6 and 7	1.2	–	28	–	ns
			2.7	1.5	5.9	9.5	ns
			3.0 to 3.6	1.5	4.3 ⁽¹⁾	8.2	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to An; OE to Bn	see Figs 6 and 7	1.2	–	12.0	–	ns
			2.7	1.5	3.8	6.9	ns
			3.0 to 3.6	1.7	3.4 ⁽¹⁾	5.9	ns
t _{sk(0)}	skew	note 2		–	–	1.0	ns
T_{amb} = -40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nAn to nYn	see Figs 5 and 7	1.2	–	13	–	ns
			2.7	1.5	4.5	9.5	ns
			3.0 to 3.6	1.5	3.6 ⁽¹⁾	8.0	ns
t _{PZH} /t _{PZL}	3-state output enable time nOE to nYn	see Figs 6 and 7	1.2	–	20	–	ns
			2.7	1.5	5.9	12.0	ns
			3.0 to 3.6	1.5	4.3 ⁽¹⁾	10.5	ns
t _{PHZ} /t _{PLZ}	3-state output disable time nOE to nYn	see Figs 6 and 7	1.2	–	10	–	ns
			2.7	1.5	3.8	9.0	ns
			3.0 to 3.6	1.7	3.4 ⁽¹⁾	7.5	ns
t _{sk(0)}	skew	note 2		–	–	1.5	ns

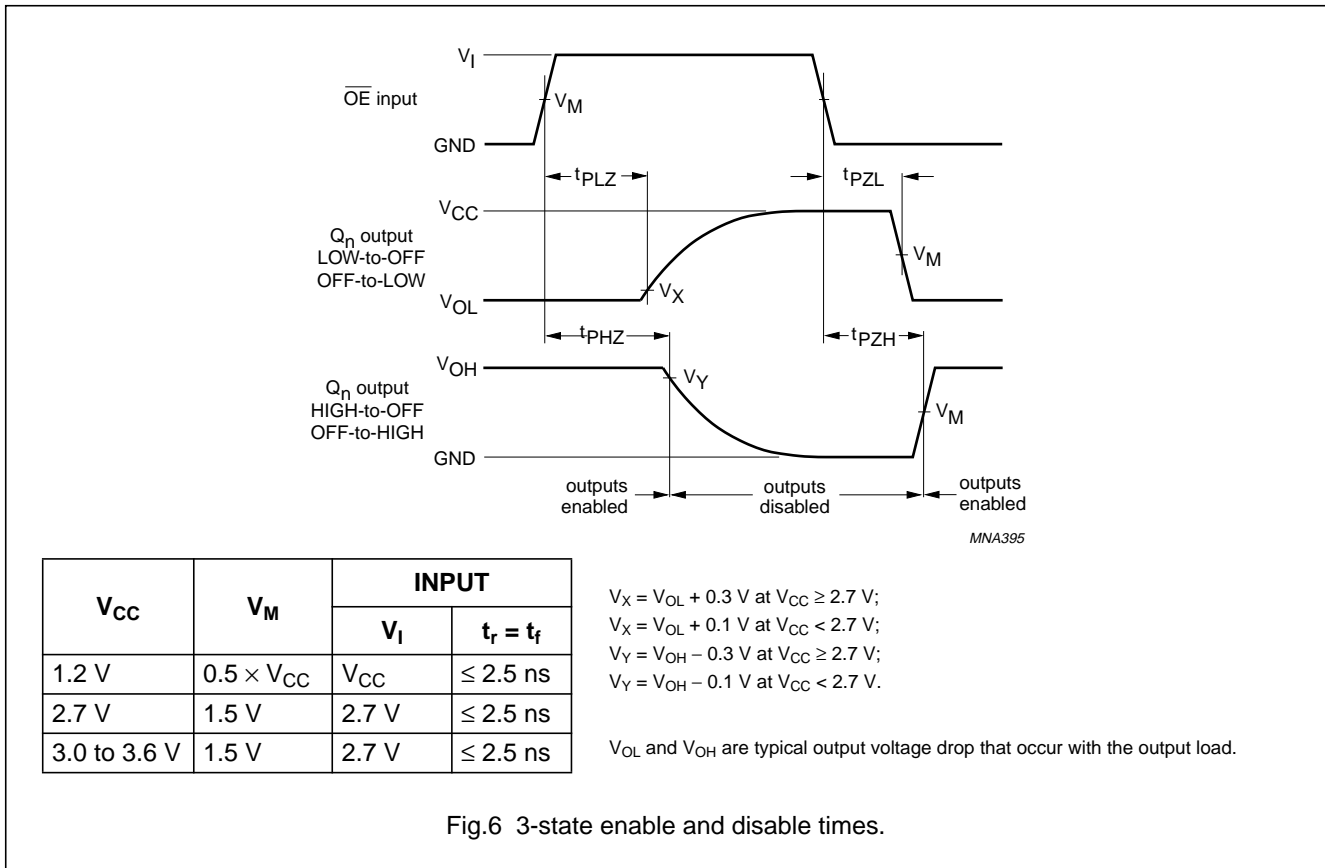
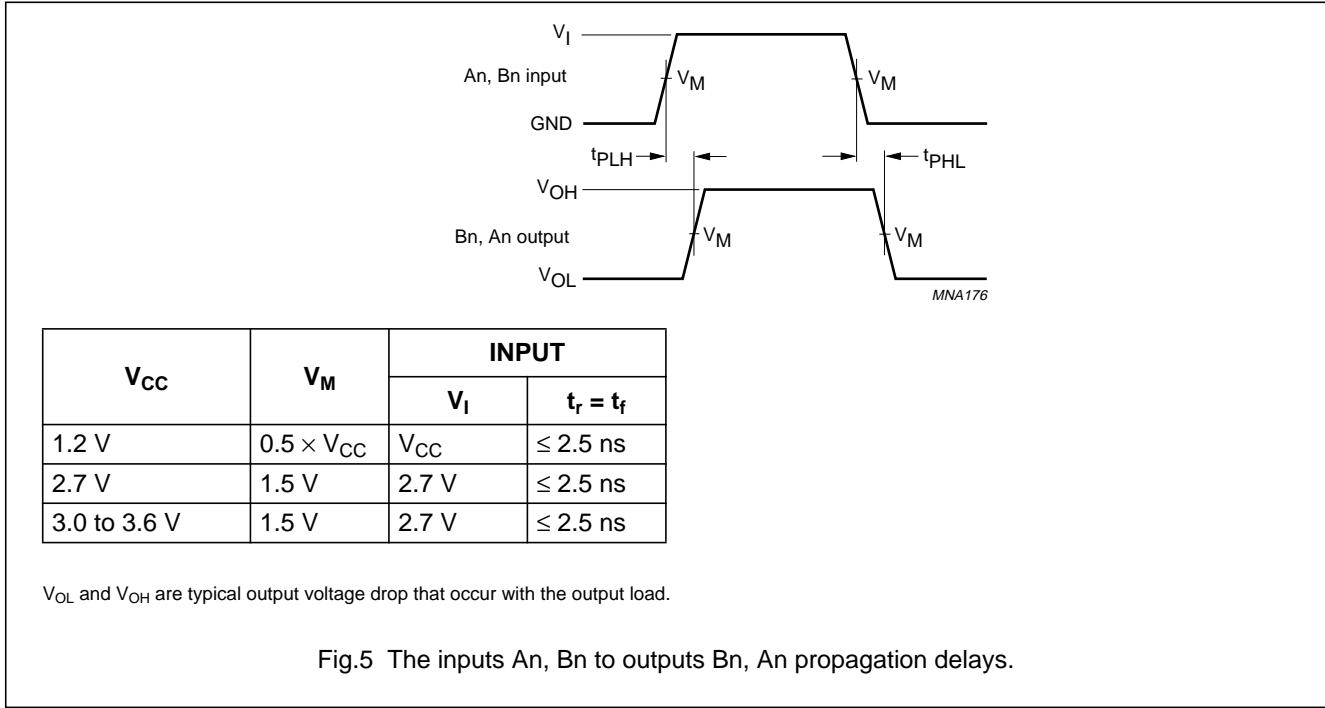
Notes

1. Typical values are measured at V_{CC} = 3.3 V.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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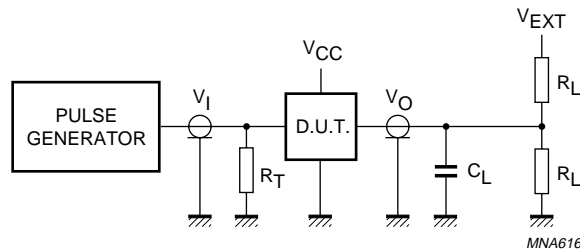
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AC WAVEFORMS



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V _{CC}	V _I	C _L	R _L	V _{EXT}		
				t _{PLH} /t _{PHL}	t _{PZH} /t _{PHZ}	t _{PZL} /t _{PLZ}
1.2 V	V _{CC}	50 pF	500 Ω ⁽¹⁾	open	GND	2 × V _{CC}
2.7 V	2.7 V	50 pF	500 Ω	open	GND	2 × V _{CC}
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V _{CC}

Note

1. The circuit performs better when R_L = 1000 Ω

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

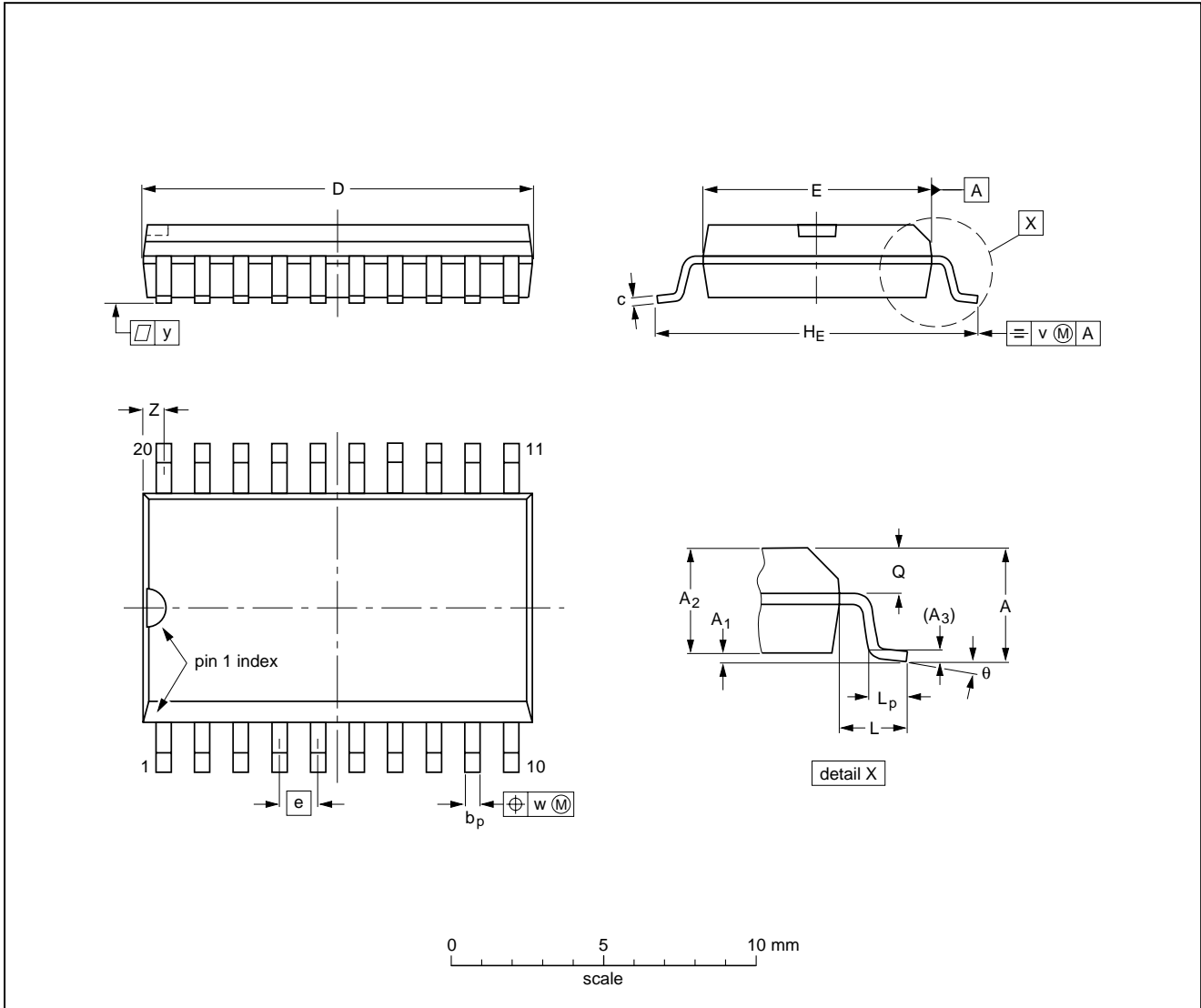
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PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

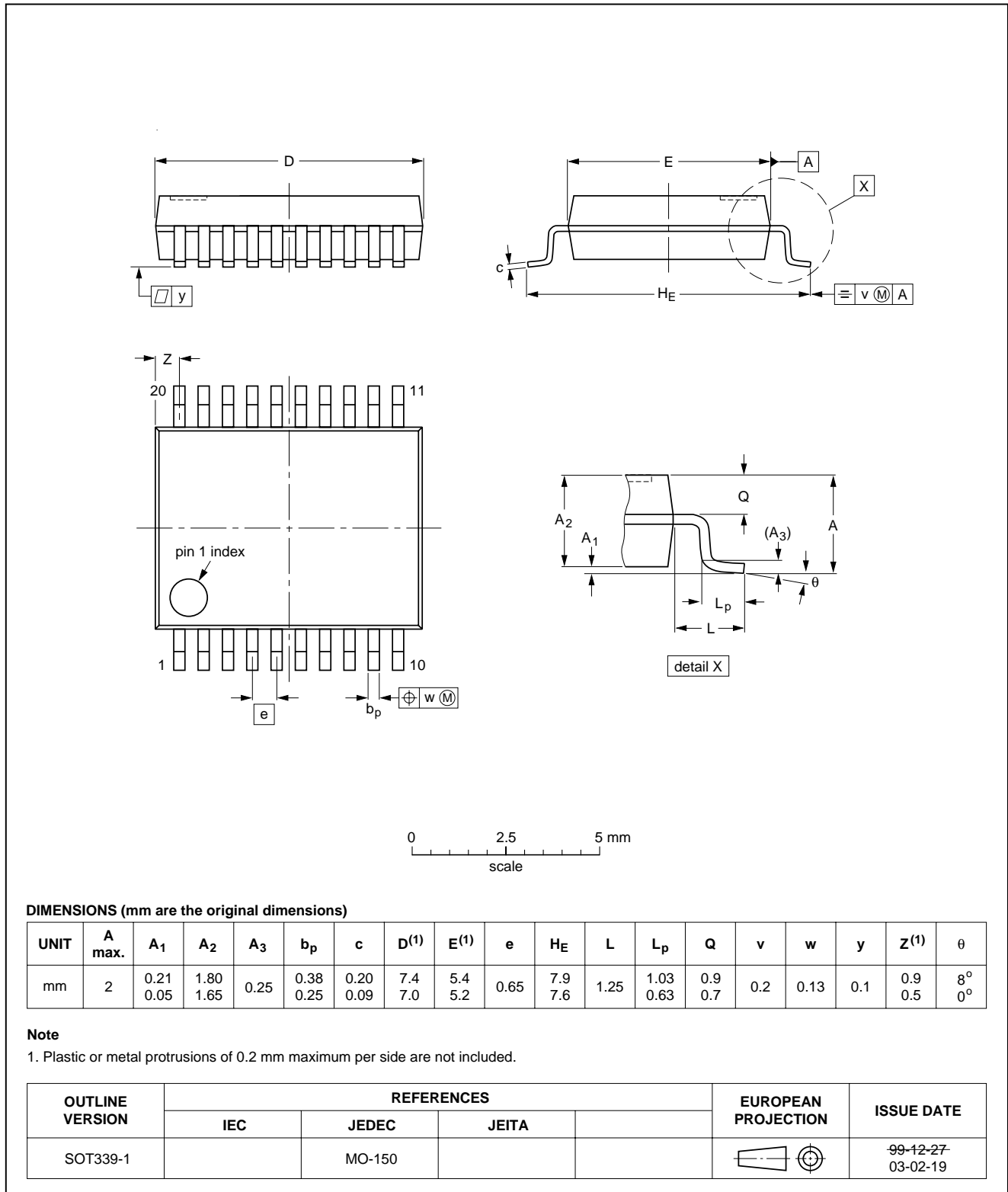
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

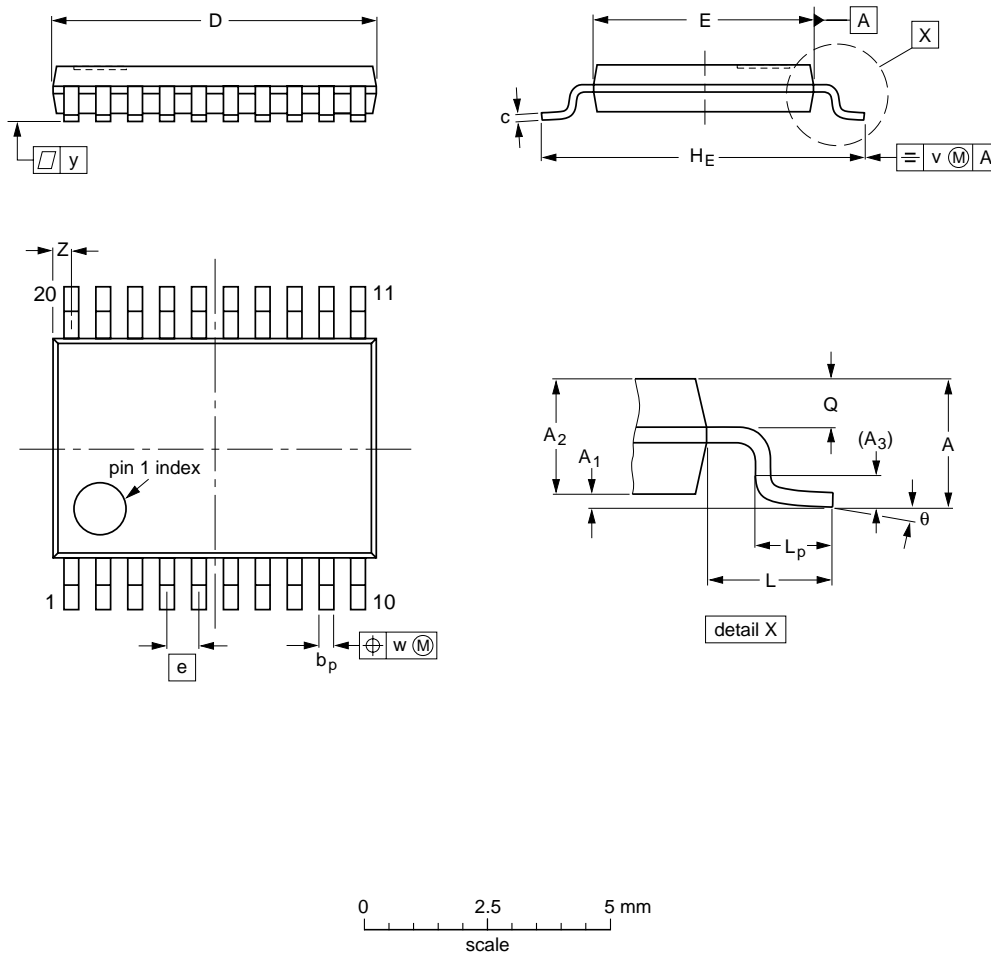


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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

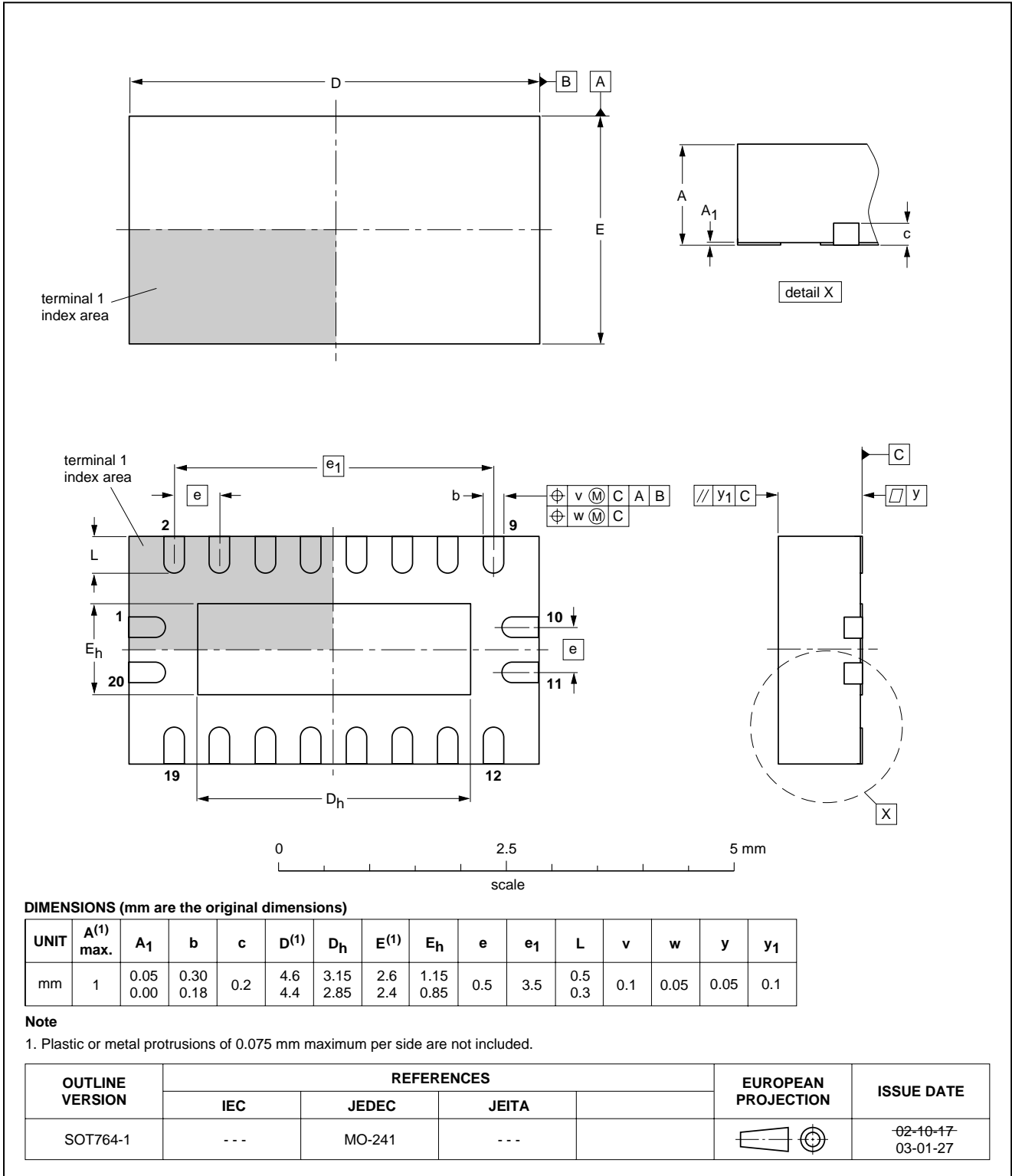
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	IEC	JEDEC	JEITA			
SOT360-1		MO-153				99-12-27 03-02-19

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DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

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